

**CLAIMS**

1. A method comprising:

causing a device including a plurality of memory cells to be programmed with asymmetric transition times between at least two states by exclusively transitioning a plurality of said cells from a first state having a longer transition time to achieve to a second state having a shorter transition time to achieve.

2. The method of claim 1, further comprising setting each of said plurality of memory cells to the first state prior to said programming.

3. The method of claim 1, wherein each memory cell includes a phase change material.

4. The method of claim 3, wherein the phase change material comprises a chalcogenide alloy.

5. The method of claim 3, wherein said transitioning comprises heating each of said memory cells.

6. The method of claim 5, wherein said heating comprises activating an electrically addressable transistor in a memory cell.

7. The method of claim 5, wherein said heating comprises directing an energy beam to a memory cell.

8. The method of claim 1, further comprising:  
determining if the device has been written to; and  
setting an indicator to a used status in response to  
determining that the device has been written to.

9. A method comprising:  
setting a plurality of memory cells in a zone of a  
memory device with asymmetric transition times between at  
least two states to a first state having a transition time  
to achieve; and  
programming the zone by exclusively transitioning  
cells from the first state to a second state having a  
shorter transition time to achieve.

10. The method of claim 9, further comprising:  
receiving a command to set memory cells in the zone to  
the first state; and

setting said memory cells to the first state.

11. The method of claim 9, further comprising setting the memory cells to the first state after a first use of the device.

12. The method of claim 10, further comprising: receiving an indication that the memory device is preparing to initiate a data download; and

setting said plurality of memory cells in the zone to the first state.

13. An apparatus comprising:  
a writer unit operative to write data to a memory device having an asymmetric transition time between two memory states, wherein a transition from a first memory state to a second memory state takes longer than a transition from the second memory state to the first memory state; and

a controller operative to control the write unit to write exclusively to memory cells to be transitioned to the first memory state.

14. The apparatus of claim 13, wherein the apparatus comprises a non-volatile phase change memory device.

15. The apparatus of claim 13, further comprising a reader unit operative to determine if a use of the apparatus is a first use, wherein the controller is operative to control the write unit to write exclusively to memory cells to be transitioned to the first memory state in response to determining that the use is the first use.

16. The apparatus of claim 13, wherein the controller is operative to control the write unit to reset a plurality of memory cells in a zone to the second memory state.

17. The apparatus of claim 16, wherein the controller is operative to control the write unit to write exclusively to memory cells in the zone.

18. The apparatus of claim 13, wherein the write unit comprises a controller operative to selectively control electrically transistors in said plurality of memory cells.

19. The apparatus of claim 13, wherein the write unit comprises an optical disc writer.

20. An article comprising a machine-readable medium including machine-executable instructions, the instructions operative to cause a machine to:

cause a device including a plurality of memory cells to be programmed with asymmetric transition times between at least two states by exclusively transitioning a plurality of said cells from a first state having a longer transition time to achieve to a second state having a shorter transition time to achieve.

21. The article of claim 20, further comprising instructions operative to cause the machine to set each of said plurality of memory cells to the first state prior to said programming.

22. An article comprising a machine-readable medium including machine-executable instructions, the instructions operative to cause a machine to:

set a plurality of memory cells in a zone of a memory device with asymmetric transition times between at least two states to a first state having a transition time to achieve; and

program the zone by exclusively transitioning cells from the first state to a second state having a shorter transition time to achieve.

23. The article of claim 22, further comprising instructions operative to cause the machine to:

receive a command to set memory cells in the zone to the first state; and

set said memory cells to the first state.

RECORDED - 2024 FEB 22 PM 11:54:20